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TECHNOLOGY, DESIGN AND MANUFACTURE OF RF SiP

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Abstract

This paper reviews the technologies, the design tools and the manufacturing resources that are available for RF Systems in a Package (RF SiP). In order to minimise the overall system costs and development times it is important to apply a rigorous methodology throughout the design process. The different steps of the process are described, starting from technology choice, through system and detailed design to manufacture.

Introduction

RF systems are notoriously difficult to design and integrate into complete applications. End users and OEMs would prefer to buy a fully tested, complete RF system as one module or package to reduce development time and manufacturing issues. Since it is often impractical to integrate the complete RF system in a single chip (SoC) the option to create a module in a package is extremely attractive.

RF System in a Package: a Definition

The so-called System in a Package (SiP) allows the integration of different semiconductor technologies together with passive functions in a single functional module. SiP may be defined as a system that has the physical form and dimensions of a semiconductor package, whilst including surface mount passive components, one or more semiconductor die and buried functionality within the substrate of the package. The complete system is protected with either a plastic over-moulded case or a combination of this and a metal shield for electromagnetic purposes.

RF SiP: Role in the product lifecycle

The product life cycle of most systems begins with a phase in which the system functionality is obtained with a large number of individual generic components mounted on a printed circuit board. At this stage the goal is to achieve technical functionality in a short time with little regard to the overall size of the system. For typical RF systems (Bluetooth and WLAN) this approach has led to Printed Circuit Board implementations of the order of 50 x 50 mm.

The next phase involves the reduction in the number of individual components mounted on the PCB, achieved mostly by the development of application specific chip-sets. Typical implementations of the order of 30 x 30 mm are achieved at this stage.

The third phase is a further increase in the integration level by mounting all the components within a single package (SiP). This is often the final form of the system as it is often impractical or impossible to achieve complete system integration on a single chip (SoC), particularly in RF applications where passive functions and technology mixes are ubiquitous.

The overall size of the SiP is of the order of 10 x 10 mm.

The final stage of system implementation, which would probably yield the lowest size and asymptotic cost, is a System on Chip (SoC) approach. Typical SoC size is of order of 7 x 7 mm.

It may be noted that the choice of SiP or SoC for any given system will depend on many parameters. These include time to market, development costs, expected production volumes, functional specifications, required product flexibility and tradeoffs between digital and RF semiconductor technologies.

There is much debate today concerning the choice of SiP versus SoC for high volume applications[1,2]. However SiP is a market-place reality today and will continue to occupy an important place in the industry for the foreseeable future.

The table below compares SiP and SoC options:

Parameter	SiP	SoC
Time to market	1 year	2 – 3 years
Technology mix Different semi-conductor processes and other components.	Yes *(includes filters and Crystals)*	No
Typical Size (mm)	10 x 10 x 1.5	7 x 7 x 0.9
Need of external components	No	Yes
Development cost	Medium	High
Production cost	Low	Very low in high volume

RF SiP Technologies

A number of SiP technologies co-exist in the market today. The main ones use multi-layer circuit boards made of either organic materials ("laminate") or Low Temperature Co-fired Ceramic materials ("LTCC"), as the substrate.

The package substrate has four major functions: interconnection between the system elements, interface to the next level of integration (PCB bumps or pads), mechanical integrity and RF passive functionality (filtering and coupling).

A further variant that is showing increasing interest amongst the Semiconductor vendors is the use of a "low cost" thin-film-on-silicon process to realize RF passive functions and interconnections between active flip chips. This silicon substrate is either packaged within a standard QFN or BGA plastic package using a laminate substrate or acts as the package for direct mounting to the mother board.

Semiconductor die are usually flip-chip mounted onto the substrate (some still use die attach/wirebond) whilst other external components are assembled using surface mount technology.
The choice of laminate, LTCC or passive Silicon technology depends on the system requirements and component mix.

Laminate will be the best choice for systems in which little or no RF passive functionality is required. However, the superior qualities of ceramic materials allow for easy integration of RF functions in the substrate and lead to the smallest form factors in such cases. The use of passive silicon substrates also allows for easy integration of RF functions but may require a second level of laminate packaging for the integration of high value capacitors, SAW devices and Crystals.

Laminate based SiP

A laminate based RF SiP uses a multi-layer organic substrate based on FR4 PCB technology. In order to improve performance at RF frequencies low dielectric loss substrates are often preferred (BT or Gtek© being 2 common choices).

Typical substrates use 4 metal layers with either one or two cores and an overall thickness of 0.4mm.

Such structures allow the integration of some RF matching structures and broadband components such as baluns within the substrate. However the majority of the RF passive functionality is obtained by the use of small SMT capacitors, inductors, resistors and integrated filters/baluns. The basic functionality of the substrate is an interconnection medium.

The technology can integrate flip-chip or wire-bonded semiconductor dice of differing technologies, ceramic filters, SAW and BAW devices and Crystals to achieve complete system functionality (digital to antenna with no external components).

The SiP is usually protected by a plastic over-mold that protects the individual components and provides a flat surface for pick and place and marking.

This technology is quite mature and is available from a range of independent suppliers using quasi-standard design rules and processes.

LTCC based SiP

Low Temperature Co-fired Ceramic (LTCC) SiP uses a multi-layer ceramic substrate. The low dielectric loss factor, high dielectric constant and fine-pitch design rules allow for the realization of much RF passive functionality within the substrate (capacitors, inductors, matching, filters and baluns).

The substrate also acts as an interconnection medium and is well suited to flip chip mounting due to the excellent match of CTE between semiconductors and ceramics.

Other components such as high value capacitors and inductors, SAW and BAW devices and Crystals are mounted on the LTCC using SMT.

The SiP is protected either with a special plastic over-mold or by a combination of glob-top/under-fill for the active components and a metal lid to protect the remaining components and furnish a flat surface for marking and pick and place.

Integrated Passive Devices

Integrated Passive Devices (IPD) offer a further route to SiP integration. The basic principle of IPD is the use of a relatively low-cost thin-film process for the creation of resistors, capacitors, inductors and interconnection patterns. The use of glass, silicon and GaAs substrates are all potential candidates for IPD.

IPDs can be used to create stand-alone RF passive functions that are integrated into a SiP using a second substrate (discrete IPD). Alternatively they can be used to form the backbone of the SiP that is then packaged as a single die (full IPD). Both Philips and SyChip have recently reported RF SiP solutions using the latter approach.

The incorporation of SAW/BAW devices, Crystals and high value capacitors and inductors may require the combination of IPD and substrate packaging techniques (laminate or LTCC) to achieve full system integration.

Design Methodologies for SiP

Design of SiP is notoriously difficult since it requires inter-working between semiconductor, packaging and PCB design concepts. The optimisation of the process is crucial to gaining the maximum benefit from the technology in terms of performance, size, cost and time to market[3,4].

The design process for RF SiP can be split into three phases:

- Feasibility, system partitioning and choice of technology.
- Design of individual functional RF blocks that are to be created within the substrate and choice of the other components.
- Routing and verification of overall performance with parasitics. This final step leads to substrate and module design definition for prototyping.

Feasibility and system partitioning

The initial choice of system partitioning and technologies is critical in determining the cost and size of the final SiP. It is crucial to evaluate all the available options from semiconductor technologies (CMOS, RF CMOS, GaAs, etc), substrates (Gtek, BT, FR4, LTCC, full IPD), assembly technologies and other passive components including SAW devices and discrete IPDs.

This stage of the design process relies heavily on the experience and know-how of the SiP and semiconductor design teams working in close cooperation. For each option the surface areas and layer structure of the substrate must be estimated together with the semiconductor technologies and areas so as to estimate overall SiP size and cost.

Design of Individual Functional Blocks

As system complexity increases, it is more and more critical to have design methodologies that take into account all levels of system design. The EDA community has focused strongly on design tools and flows for semiconductors since there is very little possibility of adjusting a design once tape-out has been completed. Furthermore, the cost of prototype runs is very high. Thus, this part of the design process is under control.

The key to successful SiP design lies in the ability to design the passive RF functions that will be incorporated in the substrate with close to “first-pass-design-success”.

Standard EDA tools

Despite the existence today of a range of system, schematic, circuit simulation, physical layout and electromagnetic tools, no one tool offers a complete end-to-end solution. In particular the design of buried RF functions within a multi-layer substrate (laminate or LTCC) requires a flexible approach that is not too dependent on a particular layer structure. This is radically different from the library methods adopted for semiconductor design, in which a given technology has a fixed layer structure.

Design of Buried RF Functions

Buried RF functions can be taken to include such elements as matching networks, filters, baluns, and RF decoupling.

Insight RF has put together a design methodology that uses standard EDA packages to achieve rapid and flexible design of such buried RF functions in multi-layer substrates.

The methodology is broken down into a number of steps to allow the designer to progressively transfer circuit elements to a fully validated 3-D layout:

- Schematic design of each RF function using simple lumped and distributed components (using elements from a circuit simulator with optimisation to functional goals)
- Initial choice of a substrate layer structure (materials, thickness, ground plane and signal layers).
- Use of a library of parameterised mechanical objects that are projected onto the layer structure. This library can be enriched during the design to create new shapes that may be necessary. Creation of parameterised schematic objects that correspond to the layout objects using electromagnetic simulation.
- Schematic design using layout objects as defined previously (uses the circuit simulator with optimisation and potential co-simulation with active devices).
- Automatic layout creation.
- RF functional block verification using 3-D electromagnetic simulation of the complete layout.
- Fine tuning of layout to close the loop between circuit and layout using circuit optimisation only (no optimisation at the layout level is required).

The design of RF passive functions using IPD is carried out using a pre-determined library approach since the layer structure is fixed and foundry dependent.

System integration and final layout

The final stage of the SiP design process is to integrate all the individual functions and complete a full layout of the module.

A number of alternative tool sets can be used for this step, each having a different set of tradeoffs. For full system SiP (digital to RF) the routing complexity and the need for co-simulation require a high level tool that can handle semiconductor design, SiP and PCB. For lower complexity modules such as RF PA and front-end only modules, the use of a circuit and electromagnetic simulator package is more flexible

Whichever tool class is chosen it is important to carry out a full system verification to ensure that the routing does not create any un-wanted parasitics.

The overall process ensures that the complete system has the maximum probability of meeting its specifications after a minimum number of design loops.

Manufacturing of SiP

In order to meet the objectives of time to market and overall production costs it is important to match manufacturing resources to the proposed SiP at the initial stages of the design. There now exists a complete range of Asian suppliers for the SiP market.

Substrates

LTCC substrates are available from a range of suppliers having quite similar design rules. Typical layer thickness varies from 20 to 200 um, via diameter is typically in the 100 um range, whilst minimum line-width and line-space is 100 um. The total number of layers determines the overall cost and can vary from 4 to 50. Buried and blind vias are a natural product of the LTCC process.

Laminate suppliers also offer a range of materials and layer thickness at typically lower cost per layer and per mm^2. However the use of buried and blind vias impact the cost negatively. Since the laminate material properties are less well controlled than those of LTCC it is more difficult to integrate narrow-band RF functions.

Thin film IPD substrates are less freely available in the open market than either laminate or LTCC. Currently this technology is proposed by one major assembly sub-contractor[5] but is more widely used internally by certain semiconductor companies (Philips, ST, etc).

Assembly

The main packaging sub-contractors and in-house lines are now able to handle both laminate and LTCC based SiP with fine-pitch flip chip die. They also have qualified techniques for over-molding and metal shielding of SiP.

The assembly of IPD based solutions relies on the similarities between the substrate and active circuit silicon. Flip chip and wire-bond assembly methods are used to package such devices as for semiconductor die.

Test

The final phase of product manufacture is complete functional testing. The test sub-contractors that are used to working on complex single package die are equally capable of handling SiP solutions, as the test vectors and handling are similar.

Conclusions

This review of RF SiP shows that there are no fundamental difficulties in achieving cost and size optimal solutions. However to achieve this it is necessary to consider all the options for each project and to use carefully chosen design methodologies matched to available manufacturing capabilities.

References

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