Sophia Antipolis
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Session 4: Mixed Signal RF

Technology, Design and Manufacture of RF SiP

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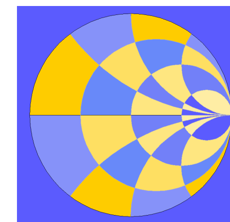


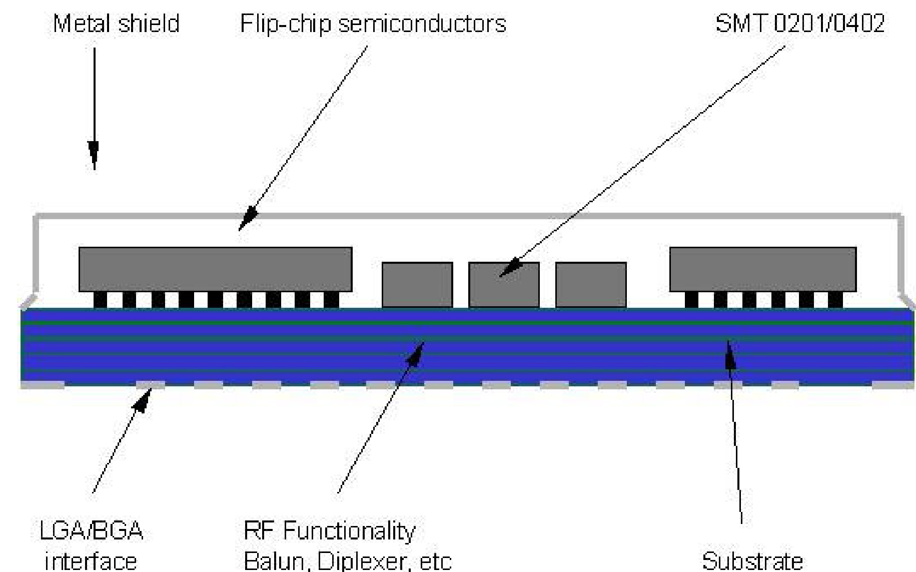
Insight SiP

Summary

- **Introduction**
  - Definition of RF System in Package (RF SiP)
  - Role of RF SiP in product life-cycle
- **RF SiP Technologies**
  - Laminate based SiP
  - LTCC based SiP
  - Integrated Passive Devices
- **Design Methodologies for SiP**
  - Feasibility and System Partitioning
  - Standard EDA Tools
  - Design of Buried RF Functions
  - System Integration and Final Layout
- **Manufacturing of SiP**
  - Substrates
  - Assembly
  - Test
- **Conclusions**

Introduction (SiP versus SoC)

- **System on Chip versus System in Package**
  - To SiP or to SoC?
  - SoC = System on Chip : as much of a system that can be designed in ONE semiconductor technology.
- **What is RF SiP?**
  - A complete RF solution including:
    - One or more semiconductor die
    - RF passive functionality (buried in substrate and/or in SMTs)
    - Physical form of a semiconductor package
    - Fully tested sub-system



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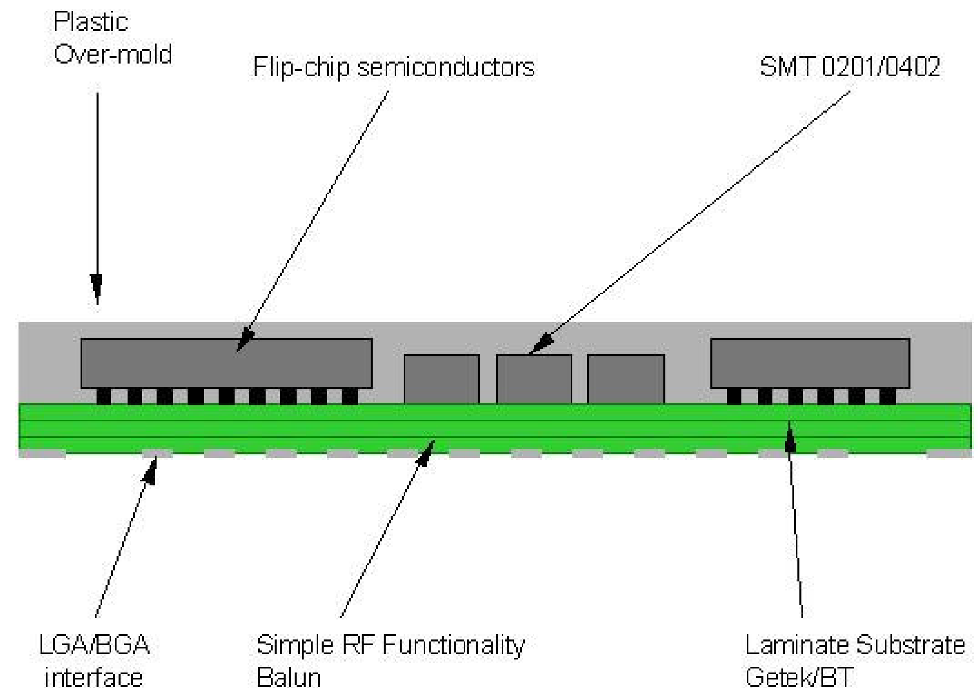
Role of RF SiP in product life-cycle

- **RF system life-cycle**
  - PCB many components 50 x 50 mm. Functionality.
  - Reduction in PCB area by reduced BoM. 30 x 30 mm
  - Initial SiP 10 x 10 mm
  - Complete SoC 7 x 7 mm
- **SiP vs SoC**
  - SiP can realize complete RF sub-system
  - SoC needs at least external passives
  - SoC could be lowest cost in high volumes

Parameter	SiP	SoC
Time to market	1 yr	2 – 3 yrs
Technology mix	Yes Filters/Xtal	No
Typical size	10 x 10 x 1.5 mm	7 x 7 x 0.9 mm
Need for ext components	No	Yes
Development cost	Medium	High
Production cost	Low	Very low

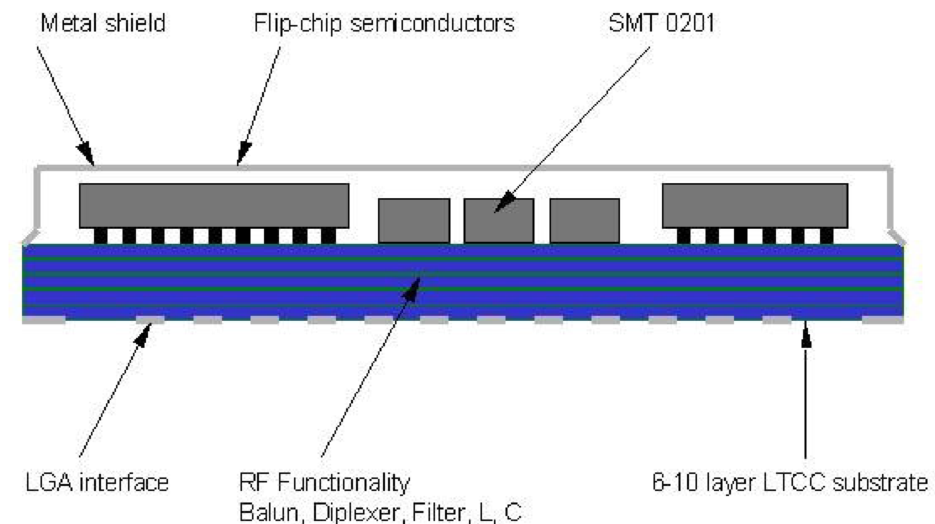
Laminate based SiP

- **Multi-layer Substrate**
  - Getek, BT
  - Typical 4 metal layers
  - 2 cores or single core
  - Total thickness ca 0.4 mm
- **Functionality - substrate**
  - Interconnection, module interface
  - Wideband passives (baluns, filters)
- **Functionality - SMT component**
  - Filters, Xtals, SAW, L, C, R
- **Functionality - semiconductors**
  - Flip chip (or wire-bond)
- **Protection**
  - Plastic over-mold
  - Metal lid for shielding



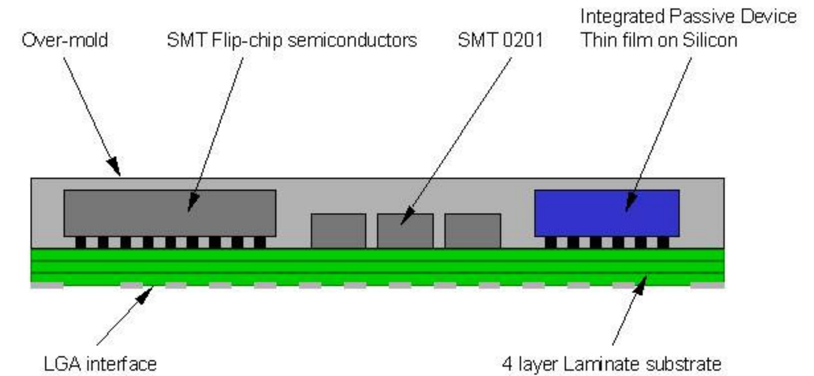
LTCC based SiP

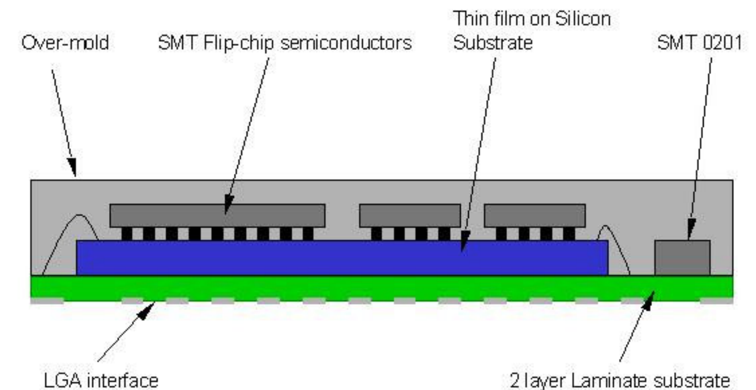
- **LTCC Substrate**
  - 6 to 10 layers
  - ε_r = ca 8
  - Total thickness ca 0.5 mm
- **Functionality – substrate**
  - Low value L, C
  - Filters, Baluns,
  - Interconnections, module interface
- **Functionality – SMT components**
  - L, C, R, Xtals, SAW
- **Functionality – Semiconductors**
  - Flip-chip or wire-bond
- **Protection**
  - Metal lid (or over-mold)



Integrated Passive Devices

- **Low-cost Thin Film Process**
  - Based on Silicon technology
  - Substrates – Glass, Si, GaAs (!)
  - Tolerances – few %
- **Functionality – thin-film substrate**
  - L, C, R, Filters, Baluns, Interconnections
- **Functionality – laminate**
  - Further interconnect
  - Module Interface
- **Functionality – semiconductors**
  - Flip-chip onto IPD or laminate
- **Portection**
  - Over-mold (and lid)





Design – Feasibility & System Partitioning

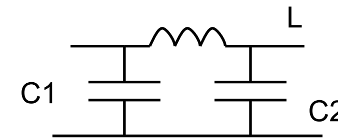
- **Semiconductor Technologies**
  - CMOS, RF CMOS, GaAs, SiGe
  - Cost, Functionality, Size, Risk
- **SiP Technologies**
  - Laminate, LTCC, Thin Film, IPD
  - Cost, Functionality, Size, Design effort, Risk
- **Assembly Technologies**
  - SMT 0201/0402
  - Flip-chip
  - Wire-bond
  - Second-level interconnect (PCB)
  - Cost, Reliability
- **Compare Technologies**
  - Based on experience & analysis

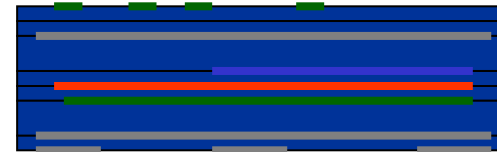
Design – Standard EDA Tools

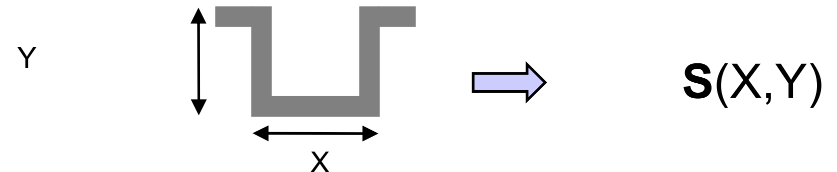
- **Range of Tools**
  - System Simulation
  - Schematic Capture and Circuit Simulation based on Library Approach
  - Automatic layout generation from library
  - Electromagnetic verification tools
- **Semiconductor Design Flow**
  - Well established and based on a library of elements for each foundry
- **Buried RF Functions**
  - Ideally should allow for optimization of layer structure during design
  - Library approach not well suited
- **Integration of SiP and SoC**
  - Currently requires the use of multiple tools
  - Industry leaders are moving towards integration of PCB, Package and Semiconductor Design Flows

Design – Buried RF Functions (1)

- **Schematic Design**
  - Standard lumped/distributed elements
  - Optimization with active devices
- **Choice of Layer Structure**
  - Materials, Thickness, Layer count
- **Generation of Parametric Objects (L, C, Lines, Baluns)**
  - Generation using flexible library of mechanical parts that are mapped to layer structure
  - EM simulation to create local library elements for each project
  - Electrical performance depends on mechanical parameters



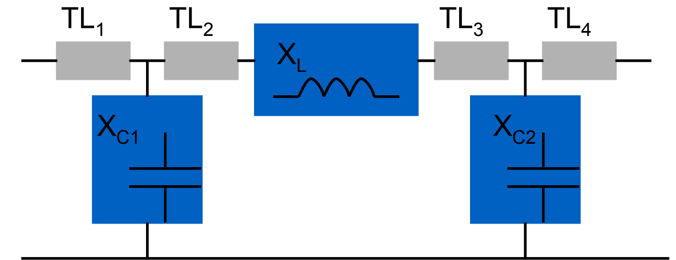


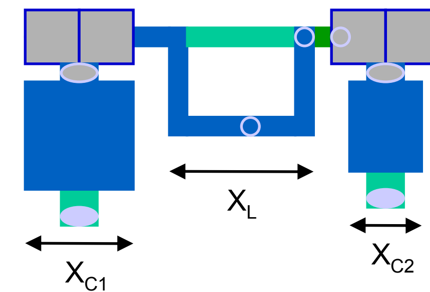


Parameters X,Y

Design – Buried RF Functions (2)

- **Optimization with Parametric Objects**
  - Replace idealized elements
  - Co-simulation with active devices
  - If necessary change layer structure and re-do
- **Automatic Layout Generation**
  - Complete buried functions
- **Electromagnetic Verification**
  - Compare to optimized results
- **Fine-tune Layout**
  - Uses optimization of the circuit model not layout.
- **Thin-film (IPD)**
  - Classical library approach may be used since layer structure is fixed by foundry





Design – System Integration and Layout

- **System Integration**
  - Active semiconductor devices
  - Buried Passive Functions
  - Other SMT devices
- **Complex systems**
  - Use of full-flow tools combining PCB, Package and Semiconductors (eg Cadence)
- **Simple systems**
  - Use of EM based tools with link to schematic (Agilent ADS, Ansoft Designer)

Manufacture - Substrates

- **Asian base of substrate manufacturers**
- **LTCC**
  - Layer thickness 20 to 100 um
  - Via diameter ca 100um
  - Line/space widths 100um
  - Buried and Blind vias
- **Laminate**
  - Range of materials, thickness, via types
  - Buried functions limited to wideband due to material tolerances
  - Lower cost per mm2 than LTCC but inferior tolerances for buried functions
- **Thin film**
  - Mostly captive (ST, Philips)
  - Cost ? Tolerances as good or better than LTCC.
  - Available from Stats ChipPac as CSMP (Chip Scale Module Package)

Manufacture – Assembly & Test

- **Assembly**
  - Sub-contractors
    - Wide range in Far East
  - Technologies
    - Wire-bond and fine-pitch flip chip
    - SMT assembly
    - Over-molding and metal lids
    - Thin film is treated as a semiconductor die (flip-chip or wire-bond)
- **Test**
  - Most assembly houses have integrated test activities
  - Other specialized test-houses exist in Far East
  - Uses same equipment as single die in package testing (handler and tester)

Conclusions

- **RF System in Package**
  - Offers a cost effective route to RF system integration
  - Development times are kept under control (cf SoC)
  - System partition and choice of SiP type need to be carefully considered for each project
  - Requires specialized design methods available today
  - A complete range of cost effective manufacturing resources exists